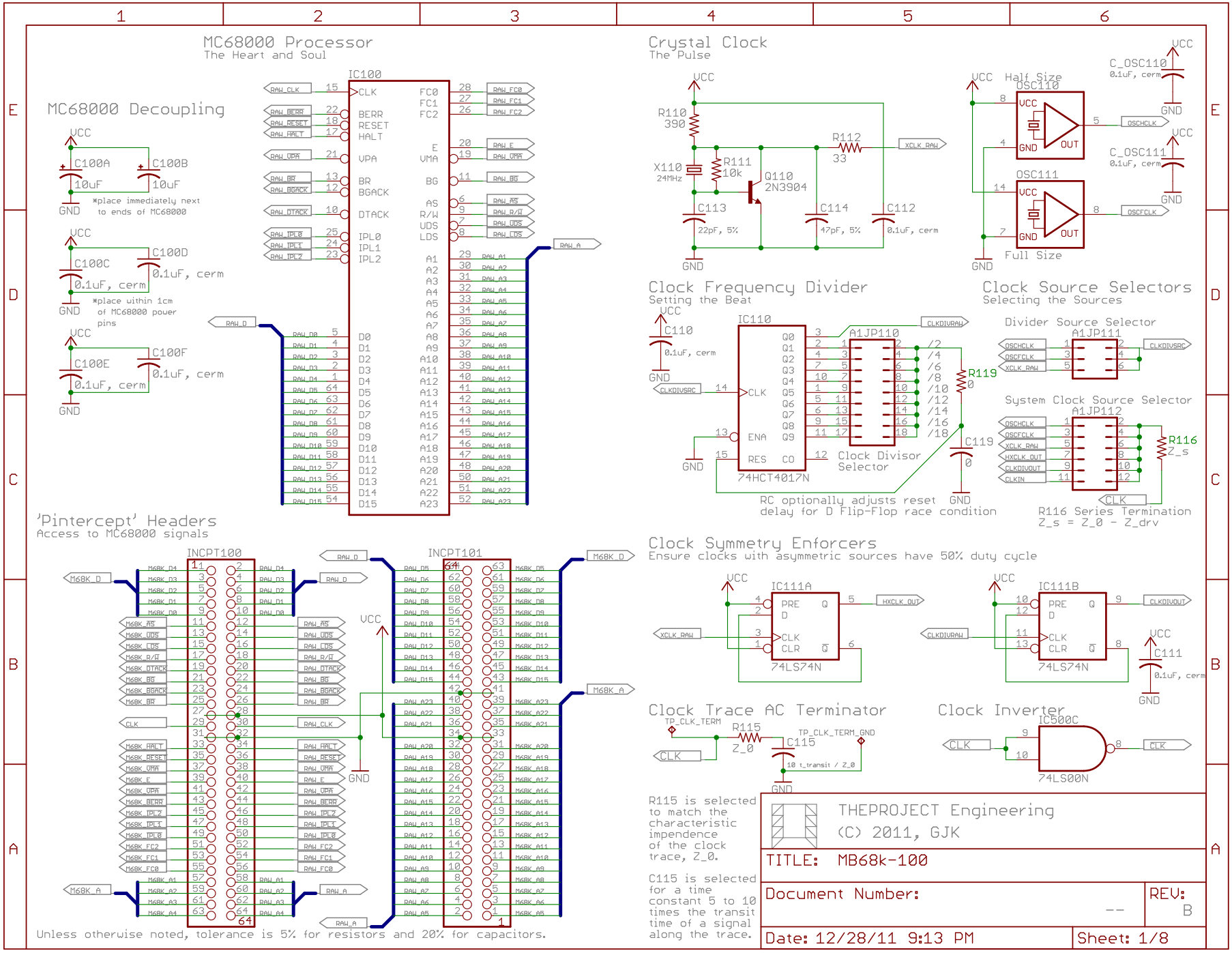
MC68000 Processor
The Heart and Soul
IC100
MC68000 Decoupling
C100A 10uF
C100B 10uF
*place immediately next to ends of MC68000
C100C 0.1uF, cerm
C100D 0.1uF, cerm
*place within 1cm of MC68000 power pins
C100E 0.1uF, cerm
C100F 0.1uF, cerm
'Pintercept' Headers
Access to MC68000 signals
INCPT100
INCPT101
Unless otherwise noted, tolerance is 5% for resistors and 20% for capacitors.
Crystal Clock
The Pulse
R110 390
X110 24MHz
R111 10k
Q110 2N3904
R112 33
C113 22pF, 5%
C114 47pF, 5%
C112 0.1uF, cerm
Half Size
OSC110
C_OSC110 0.1uF, cerm
OSC111
C_OSC111 0.1uF, cerm
Full Size
Clock Frequency Divider
Setting the Beat
C110 0.1uF, cerm
IC110
74HCT4017N
A1JP110
Clock Divisor Selector
R119 0
C119 0
RC optionally adjusts reset delay for D Flip-Flop race condition
Clock Source Selectors
Selecting the Sources
Divider Source Selector
A1JP111
System Clock Source Selector
A1JP112
R116 Z_s
R116 Series Termination
Z_s = Z_0 - Z_drv
Clock Symmetry Enforcers
Ensure clocks with asymmetric sources have 50% duty cycle
IC111A
74LS74N
IC111B
74LS74N
C111 0.1uF, cerm
Clock Trace AC Terminator
R115 Z_0
C115 10 t_transit / Z_0
Clock Inverter
IC500C
74LS00N
R115 is selected to match the characteristic impendence of the clock trace, Z_0.
C115 is selected for a time constant 5 to 10 times the transit time of a signal along the trace.
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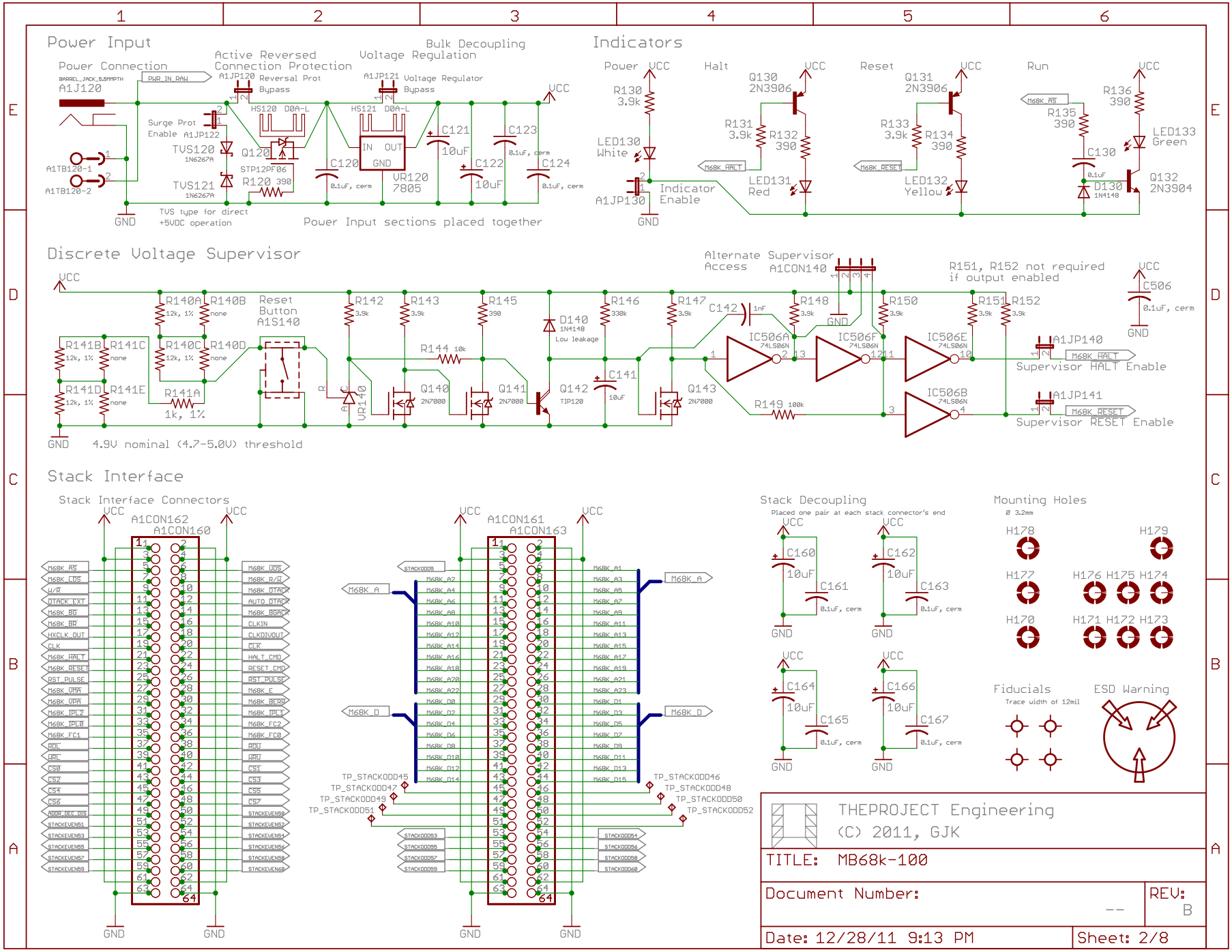
Power Input
Power Connection
A1J120
Active Reversed Connection Protection
Reversal Prot Bypass
Bulk Decoupling
Voltage Regulation
Voltage Regulator Bypass
Surge Prot Enable
TVS120
TVS121
Q120
R120 390
C120
VR120 7805
C121 10uF
C122 10uF
C123
C124
TVS type for direct +5VDC operation
Power Input sections placed together
Indicators
Power
Halt
Reset
Run
R130 3.9k
LED130 White
Indicator Enable
A1JP130
Q130 2N3906
R131 3.9k
R132 390
LED131 Red
Q131 2N3906
R133 3.9k
R134 390
LED132 Yellow
R135 390
R136 390
C130
D130 1N4148
LED133 Green
Q132 2N3904
Discrete Voltage Supervisor
Alternate Supervisor Access
A1CON140
R151, R152 not required if output enabled
C506
R140A 12k, 1%
R140B none
R140C 12k, 1%
R140D none
R141B 12k, 1%
R141C none
R141D 12k, 1%
R141E none
R141A 1k, 1%
Reset Button
A1S140
R142 3.9k
R143 3.9k
R144 10k
R145 390
D140 1N4148 Low leakage
R146 330k
R147 3.9k
C142 1nF
C141 10uF
Q140 2N7000
Q141 2N7000
Q142 TIP120
Q143 2N7000
VR140
R148 3.9k
R149 100k
R150 3.9k
R151 3.9k
R152 3.9k
IC506A 74LS06N
IC506F 74LS06N
IC506E 74LS06N
IC506B 74LS06N
A1JP140
Supervisor HALT Enable
A1JP141
Supervisor RESET Enable
4.9V nominal (4.7-5.0V) threshold
Stack Interface
Stack Interface Connectors
A1CON162
A1CON160
A1CON161
A1CON163
Stack Decoupling
Placed one pair at each stack connector's end
C160 10uF
C161 0.1uF, cerm
C162 10uF
C163 0.1uF, cerm
C164 10uF
C165 0.1uF, cerm
C166 10uF
C167 0.1uF, cerm
Mounting Holes
Ø 3.2mm
H178
H179
H177
H176 H175 H174
H170
H171 H172 H173
Fiducials
Trace width of 12mil
ESD Warning
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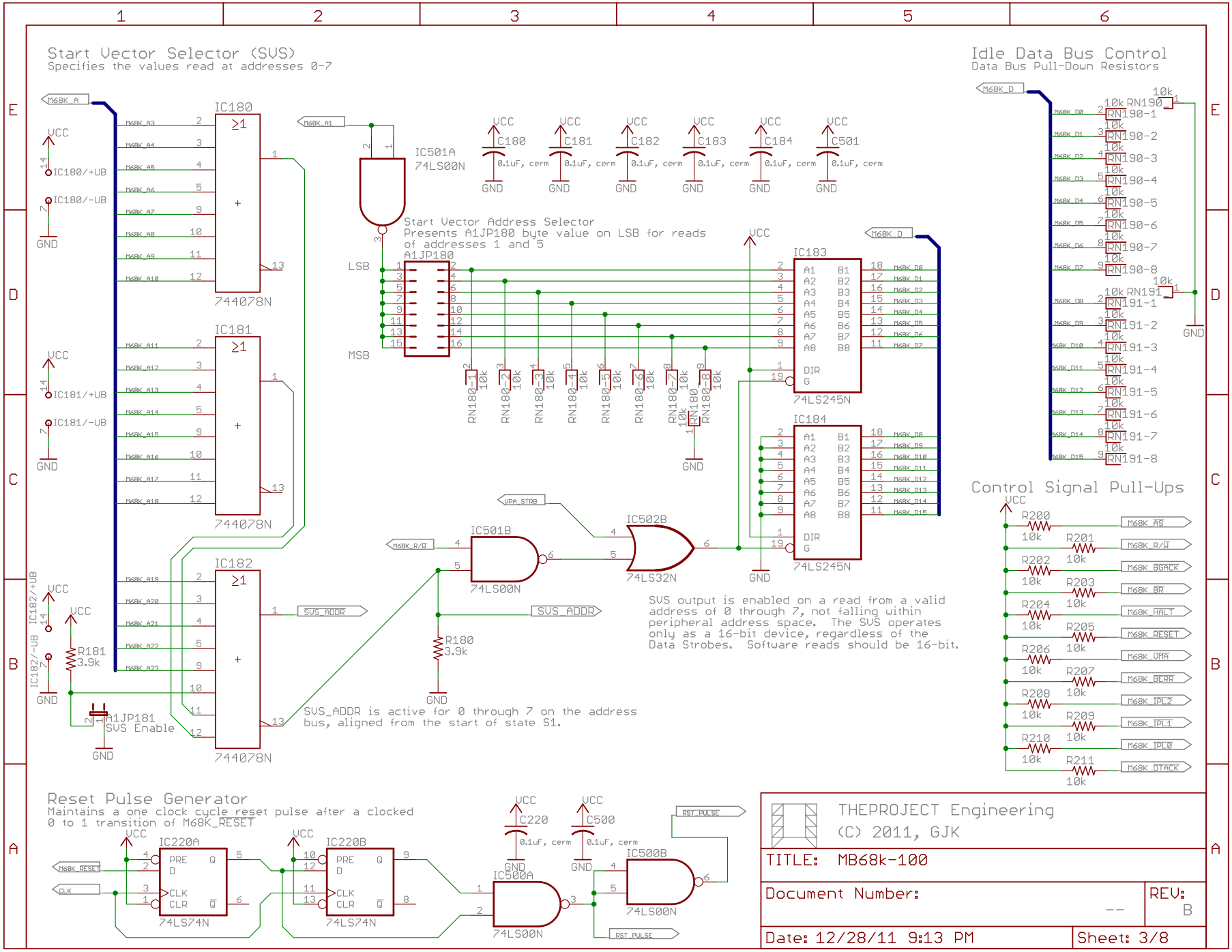
Start Vector Selector (SVS)
Specifies the values read at addresses 0-7
Idle Data Bus Control
Data Bus Pull-Down Resistors
Start Vector Address Selector
Presents A1JP180 byte value on LSB for reads of addresses 1 and 5
SVS output is enabled on a read from a valid address of 0 through 7, not falling within peripheral address space. The SVS operates only as a 16-bit device, regardless of the Data Strobes. Software reads should be 16-bit.
SVS_ADDR is active for 0 through 7 on the address bus, aligned from the start of state S1.
Control Signal Pull-Ups
Reset Pulse Generator
Maintains a one clock cycle reset pulse after a clocked 0 to 1 transition of M68K_RESET
IC180
IC181
IC182
744078N
IC501A
74LS00N
IC183
IC184
74LS245N
IC501B
IC502B
74LS32N
IC220A
IC220B
74LS74N
IC500A
IC500B
A1JP180
A1JP181
SVS Enable
LSB
MSB
VCC
GND
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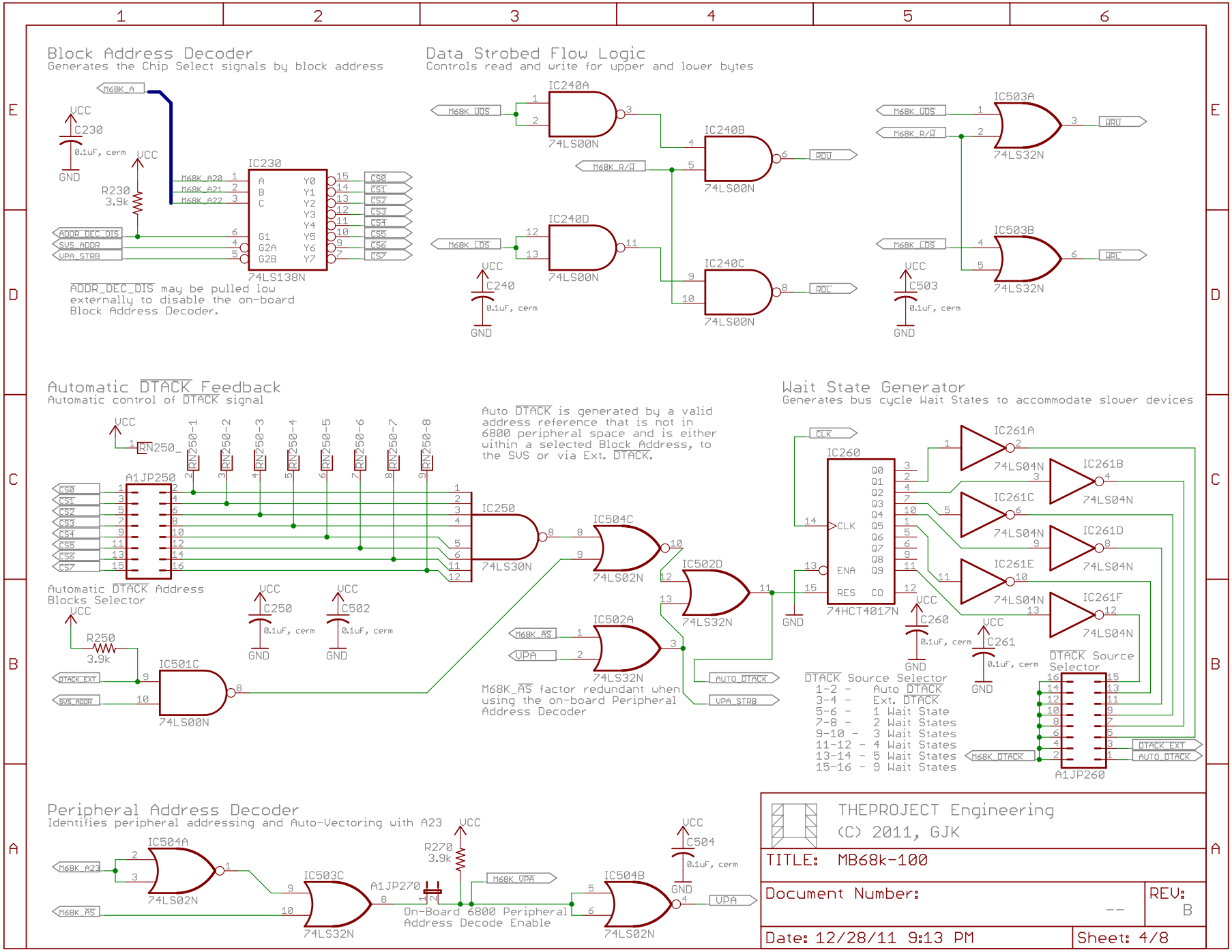
Block Address Decoder
Generates the Chip Select signals by block address
M68K_A
VCC
C230
0.1uF, cerm
GND
R230
3.9k
IC230
M68K_A20
M68K_A21
M68K_A22
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CS0
CS1
CS2
CS3
CS4
CS5
CS6
CS7
ADDR_DEC_DIS
SVS_ADDR
VPA_STRB
74LS138N
ADDR_DEC_DIS may be pulled low externally to disable the on-board Block Address Decoder.
Data Strobed Flow Logic
Controls read and write for upper and lower bytes
IC240A
M68K_UDS
74LS00N
IC240B
M68K_R/W
RDU
IC240D
M68K_LDS
C240
IC240C
RDL
IC503A
WRU
74LS32N
IC503B
WRL
C503
Automatic DTACK Feedback
Automatic control of DTACK signal
RN250_
RN250-1
RN250-2
RN250-3
RN250-4
RN250-5
RN250-6
RN250-7
RN250-8
A1JP250
IC250
74LS30N
IC504C
74LS02N
IC502D
74LS32N
IC502A
M68K_AS
VPA
AUTO_DTACK
VPA_STRB
Auto DTACK is generated by a valid address reference that is not in 6800 peripheral space and is either within a selected Block Address, to the SVS or via Ext. DTACK.
Automatic DTACK Address Blocks Selector
R250
3.9k
DTACK_EXT
SVS_ADDR
IC501C
C250
C502
M68K_AS factor redundant when using the on-board Peripheral Address Decoder
Wait State Generator
Generates bus cycle Wait States to accommodate slower devices
CLK
IC260
ENA
RES
CO
74HCT4017N
IC261A
IC261B
IC261C
IC261D
IC261E
IC261F
74LS04N
C260
C261
DTACK Source Selector
1-2 - Auto DTACK
3-4 - Ext. DTACK
5-6 - 1 Wait State
7-8 - 2 Wait States
9-10 - 3 Wait States
11-12 - 4 Wait States
13-14 - 5 Wait States
15-16 - 9 Wait States
M68K_DTACK
A1JP260
Peripheral Address Decoder
Identifies peripheral addressing and Auto-Vectoring with A23
M68K_A23
IC504A
74LS02N
IC503C
74LS32N
A1JP270
R270
3.9k
M68K_VPA
On-Board 6800 Peripheral Address Decode Enable
IC504B
C504
VPA
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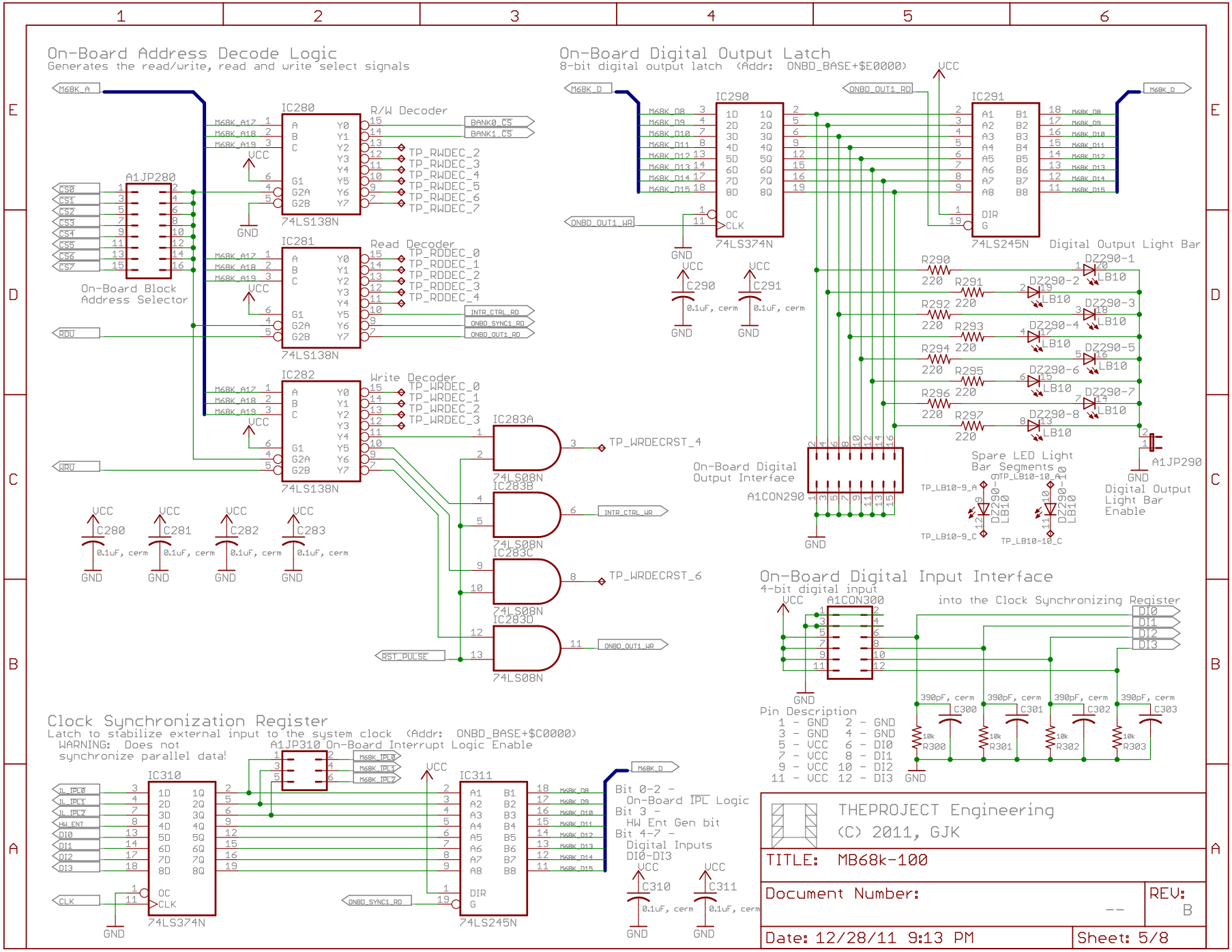
On-Board Address Decode Logic
Generates the read/write, read and write select signals
IC280
R/W Decoder
74LS138N
IC281
Read Decoder
74LS138N
IC282
Write Decoder
74LS138N
A1JP280
On-Board Block Address Selector
IC283A
IC283B
IC283C
IC283D
74LS08N
On-Board Digital Output Latch
8-bit digital output latch (Addr: ONBD_BASE+$E0000)
IC290
74LS374N
IC291
74LS245N
Digital Output Light Bar
On-Board Digital Output Interface
A1CON290
Spare LED Light Bar Segments
A1JP290
Digital Output Light Bar Enable
On-Board Digital Input Interface
4-bit digital input
A1CON300
into the Clock Synchronizing Register
Pin Description
1 - GND 2 - GND
3 - GND 4 - GND
5 - VCC 6 - DI0
7 - VCC 8 - DI1
9 - VCC 10 - DI2
11 - VCC 12 - DI3
Clock Synchronization Register
Latch to stabilize external input to the system clock (Addr: ONBD_BASE+$C0000)
WARNING: Does not synchronize parallel data!
A1JP310 On-Board Interrupt Logic Enable
IC310
74LS374N
IC311
74LS245N
Bit 0-2 - On-Board IPL Logic
Bit 3 - HW Ent Gen bit
Bit 4-7 - Digital Inputs DI0-DI3
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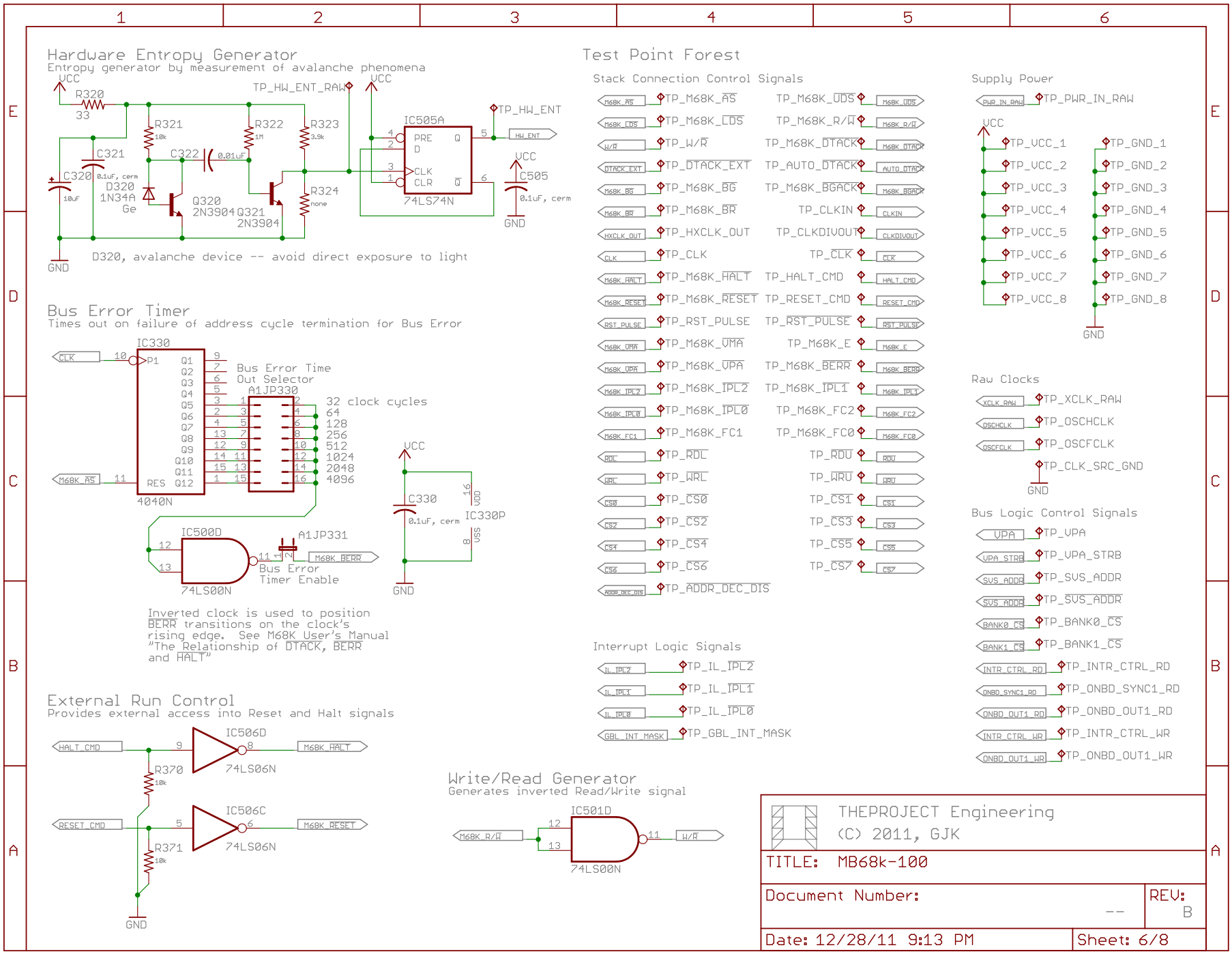
Hardware Entropy Generator
Entropy generator by measurement of avalanche phenomena
VCC
R320
33
R321
10k
R322
1M
R323
3.9k
TP_HW_ENT_RAW
VCC
IC505A
PRE
D
CLK
CLR
Q
Q̄
74LS74N
TP_HW_ENT
HW_ENT
VCC
C505
0.1uF, cerm
GND
C321
C322
0.01uF
C320
0.1uF, cerm
10uF
D320
1N34A
Ge
Q320
2N3904
Q321
2N3904
R324
none
GND
D320, avalanche device -- avoid direct exposure to light
Bus Error Timer
Times out on failure of address cycle termination for Bus Error
IC330
CLK
P1
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
M68K_AS
RES
4040N
Bus Error Time
Out Selector
A1JP330
32 clock cycles
64
128
256
512
1024
2048
4096
VCC
C330
0.1uF, cerm
IC330P
VDD
VSS
GND
IC500D
74LS00N
A1JP331
M68K_BERR
Bus Error
Timer Enable
Inverted clock is used to position
BERR transitions on the clock's
rising edge. See M68K User's Manual
"The Relationship of DTACK, BERR
and HALT"
External Run Control
Provides external access into Reset and Halt signals
HALT_CMD
IC506D
74LS06N
M68K_HALT
R370
10k
RESET_CMD
IC506C
74LS06N
M68K_RESET
R371
10k
GND
Write/Read Generator
Generates inverted Read/Write signal
M68K_R/W
IC501D
74LS00N
W/R
Test Point Forest
Stack Connection Control Signals
M68K_AS TP_M68K_AS
M68K_LDS TP_M68K_LDS
W/R TP_W/R
DTACK_EXT TP_DTACK_EXT
M68K_BG TP_M68K_BG
M68K_BR TP_M68K_BR
HXCLK_OUT TP_HXCLK_OUT
CLK TP_CLK
M68K_HALT TP_M68K_HALT
M68K_RESET TP_M68K_RESET
RST_PULSE TP_RST_PULSE
M68K_VMA TP_M68K_VMA
M68K_VPA TP_M68K_VPA
M68K_IPL2 TP_M68K_IPL2
M68K_IPL0 TP_M68K_IPL0
M68K_FC1 TP_M68K_FC1
RDL TP_RDL
WRL TP_WRL
CS0 TP_CS0
CS2 TP_CS2
CS4 TP_CS4
CS6 TP_CS6
ADDR_DEC_DIS TP_ADDR_DEC_DIS
TP_M68K_UDS M68K_UDS
TP_M68K_R/W M68K_R/W
TP_M68K_DTACK M68K_DTACK
TP_AUTO_DTACK AUTO_DTACK
TP_M68K_BGACK M68K_BGACK
TP_CLKIN CLKIN
TP_CLKDIVOUT CLKDIVOUT
TP_CLK CLK
TP_HALT_CMD HALT_CMD
TP_RESET_CMD RESET_CMD
TP_RST_PULSE RST_PULSE
TP_M68K_E M68K_E
TP_M68K_BERR M68K_BERR
TP_M68K_IPL1 M68K_IPL1
TP_M68K_FC2 M68K_FC2
TP_M68K_FC0 M68K_FC0
TP_RDU RDU
TP_WRU WRU
TP_CS1 CS1
TP_CS3 CS3
TP_CS5 CS5
TP_CS7 CS7
Interrupt Logic Signals
IL_IPL2 TP_IL_IPL2
IL_IPL1 TP_IL_IPL1
IL_IPL0 TP_IL_IPL0
GBL_INT_MASK TP_GBL_INT_MASK
Supply Power
PWR_IN_RAW TP_PWR_IN_RAW
VCC
TP_VCC_1
TP_VCC_2
TP_VCC_3
TP_VCC_4
TP_VCC_5
TP_VCC_6
TP_VCC_7
TP_VCC_8
TP_GND_1
TP_GND_2
TP_GND_3
TP_GND_4
TP_GND_5
TP_GND_6
TP_GND_7
TP_GND_8
GND
Raw Clocks
XCLK_RAW TP_XCLK_RAW
OSCHCLK TP_OSCHCLK
OSCFCLK TP_OSCFCLK
TP_CLK_SRC_GND
GND
Bus Logic Control Signals
VPA TP_VPA
VPA_STRB TP_VPA_STRB
SVS_ADDR TP_SVS_ADDR
SVS_ADDR TP_SVS_ADDR
BANK0_CS TP_BANK0_CS
BANK1_CS TP_BANK1_CS
INTR_CTRL_RD TP_INTR_CTRL_RD
ONBD_SYNC1_RD TP_ONBD_SYNC1_RD
ONBD_OUT1_RD TP_ONBD_OUT1_RD
INTR_CTRL_WR TP_INTR_CTRL_WR
ONBD_OUT1_WR TP_ONBD_OUT1_WR
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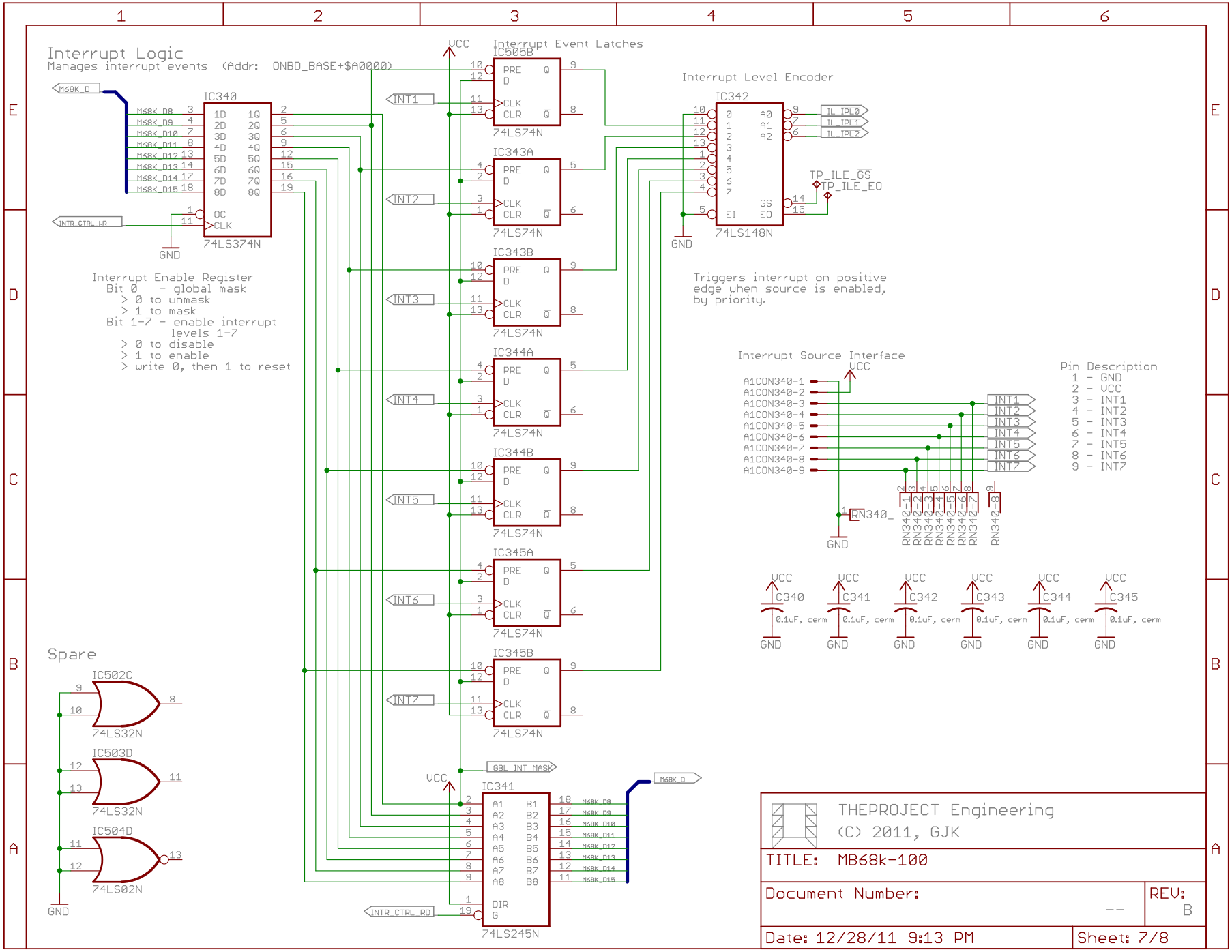
Interrupt Logic
Manages interrupt events (Addr: ONBD_BASE+$A0000)
IC340
74LS374N
Interrupt Enable Register
Bit 0 - global mask
> 0 to unmask
> 1 to mask
Bit 1-7 - enable interrupt levels 1-7
> 0 to disable
> 1 to enable
> write 0, then 1 to reset
Interrupt Event Latches
IC505B
IC343A
IC343B
IC344A
IC344B
IC345A
IC345B
74LS74N
Interrupt Level Encoder
IC342
74LS148N
Triggers interrupt on positive edge when source is enabled, by priority.
Interrupt Source Interface
Pin Description
1 - GND
2 - VCC
3 - INT1
4 - INT2
5 - INT3
6 - INT4
7 - INT5
8 - INT6
9 - INT7
Spare
IC502C
74LS32N
IC503D
74LS32N
IC504D
74LS02N
IC341
74LS245N
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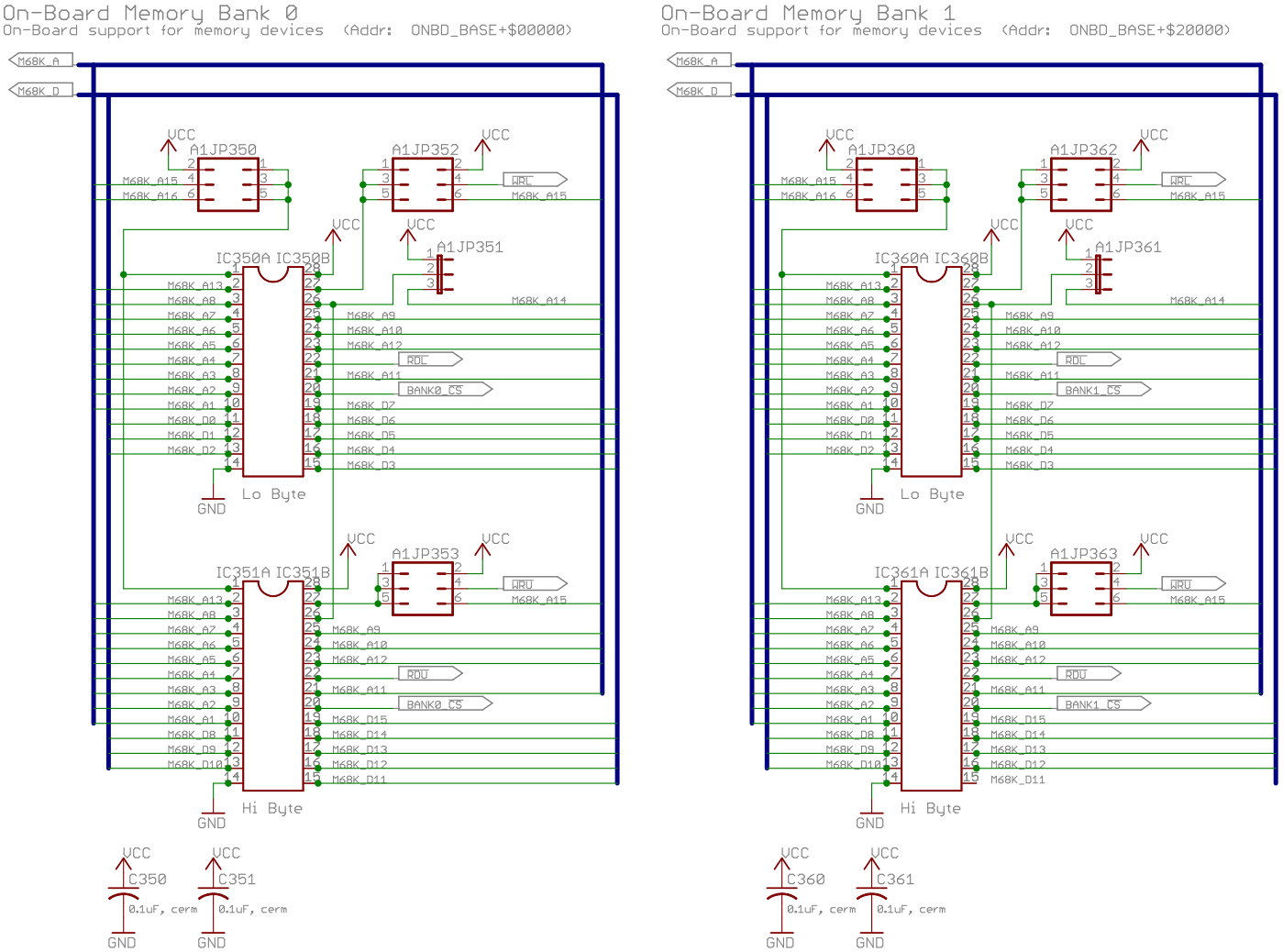

On-Board Banks support EPROM/SRAM devices according to jumper settings. EPROM device support ranges from 2732 (4kB x 2) through to 27512 (64kB x 2). Note that the 2732 device is shifted in the socket with the device's pin 1 positioned in pin 3 of the socket. With all but the 27512, address wrap-around aliasing occurs due to ignored address lines.

Jumper	Memory Device 6264	62256	2732	2764	27128	27256	27512
A1JP350,A1JP360	open	3-4	open	1-2	1-2	1-2	5-6
A1JP351,A1JP361	1-2	2-3	1-2	open	2-3	2-3	2-3
A1JP352,A1JP362	3-4	3-4	open	1-2	1-2	5-6	5-6
A1JP353,A1JP363	3-4	3-4	open	1-2	1-2	5-6	5-6

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